25.8 Low Flicker-Noise Quadrature Mixer Topology

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Flicker noise (1/*f* noise) in down-conversion mixers is a common limitation of CMOS front-ends used in direct-conversion or low-IF receivers. 1/*f* noise modulates the duty cycle of the switched mixer current, giving rise to an undesirable low frequency component that is a function of the 1/*f* noise of the quad devices, *N*9 to *N*16 of Fig. 25.8.1, and the dc current through the mixer. While previous low 1/*f* noise mixer techniques have adopted passive mixers or cancellation techniques [2], we present a new mixer topology that enables the quad to switch during periods of low or near zero currents, reducing the 1/*f* noise significantly. This topology takes advantage of the high f_t in 0.13µm CMOS or smaller gate length technologies to overcome the limitations due to 1/*f* noise. The topology also offers additional benefits of higher mixer conversion gain and lower thermal noise floor. Furthermore, excellent quadrature (I/Q) matching and lower mixer second-order intermodulation (IM2) products are obtained.

In the topology shown in Fig. 25.8.2, the current supplied to the mixer quad is modified by switching pairs *M*5-*M*6 and *M*7-*M*8, called the 2*LO stage, which are clocked at twice the nominal LO frequency. During the positive phases of 2*LO, currents from the mixer g_m stage are commutated through the drains of *M*5 and *M*7 to the I-mixer quad *M*9 to *M*12. During the negative phase of 2*LO, *M*6 and *M*8 commutate currents to the Q-mixer quad *M*13 to *M*16. The phase difference between the LO for the quads and 2*LO stage (*M*5 to *M*8) is adjusted, as shown in Fig. 25.8.3, so that transitions in the quad voltages occur when there is no instantaneous current through the quad, resulting in a significant reduction of 1/*f* noise from the mixer quad devices getting to output. The 1/*f* noise contributions of *M*5 to *M*8 convert to common-mode noise that is rejected by the subsequent differential stage. Ideally, the phase difference between the LO and 2* LO voltages should be adjusted as shown in Fig. 25.8.3 and Fig. 25.8.4. Simulations indicate that even if phase difference is not centered precisely, low 1/*f* noise is achieved as long as the 2*LO voltage transitions maintain a certain minimum delay from the quad transitions. Specifically, for the 2GHz operation demonstrated, it is seen in simulation that ±40ps of delay variation between the 2*LO waveform and LO waveforms is acceptable. Figure 25.8.2 also illustrates a simple scheme for implementing the LO signals and delays required for the topology. The extra delay through the divide by two in the upper LO path is sufficient to create the necessary timing difference.

Mixer switching waveforms can be represented as repeating pulse trains of 1010… and 1-11-1… for the 2*LO and LO signals respectively. The effective LO waveforms for the mixer, obtained by multiplying the LO signals, are shown in Fig. 25.8.4(c). For a load R_L at the output of the mixer and similar currents in both mixers, the gain of a conventional mixer is:

$$G = \left(g_{N1} + g_{N2}\right) \times \left(\frac{2}{\pi}\right) \times R_L$$

while the gain of our mixer is:

$$G = \left(g_{M1} + g_{M2} + g_{M3} + g_{M4}\right) \times \left(\frac{\sqrt{2}}{\pi}\right) \times R_L$$

The factor of √2 for our mixer comes from the Fourier expansion of the waveform of Fig. 25.8.4(c), which is identical to that of a regular mixer except for this scaling factor of –3dB. For equal currents in *M*1 to *M*4 and *N*1 to *N*4, the gain of our mixer is 3dB higher.

By shorting the drains of *N*1 and *N*3 in Fig. 25.8.1 into a single composite g_m stage, the input-referred noise contribution of *M*1 and *M*3 in Fig. 25.8.2 is improved by 3dB. *M*5 to *M*8 contribute thermal noise only at odd multiples of the LO frequency. Also, these devices are smaller than those in the quad, enabling faster switching. For similar slew rates in our topology's 2*LO buffer and in a conventional mixer's quad LO buffer, the thermal noise contributions of *M*5 to *M*8 are lower than that due to *N*9 to *N*16. Furthermore, in our topology, quad transistors act as cascode devices, contributing negligible thermal noise. For the above reasons, the thermal noise floor of our topology improves by 2.5dB.

One of the dominant IM2 mechanisms, caused by threshold mismatches in the mixer quad, is similar in principle to 1/*f* noise mechanisms. For this reason, by analogy with 1/*f* noise improvement in our topology, IM2 also improves. Simulations show that IIP2 caused by threshold mismatches in the quad improves by 10dB. Mismatches in the lower FETs are not relevant as they convert to common-mode IM2. Similar improvement is also seen in simulation when the other dominant IM2 mechanism, RF self-mixing, is considered.

In a conventional mixer, duty-cycle mismatch in the VCO buffer, or in the quadrature divide-by-two circuit, which uses relatively small FETs for high-speed operation, results in phase mismatch between the down-converted signals. As shown in Fig. 25.8.5, quad LO phase mismatches do not affect the outputs for our topology. To first order, the timing of transitions in the quad LO, which can vary due to random noise or coupling or mismatch, do not influence the operation of the mixer as long as these edges remain in the proper timing window. Any duty-cycle mismatch in the 2*LO signal, which can be minimized by ac coupling in the 2*LO path, causes a relatively small quadrature amplitude mismatch. This improves image rejection relative to a conventional mixer topology. Further, it can be shown that reciprocal mixing noise is similar to that in a conventional mixer, even though a switching stage at twice the LO frequency is used. The phase noise superimposed on the received signal is equivalent to that of the 2*LO noise attenuated by 6dB in an ideal divide-by-2 circuit. Based on the above discussion, we can also conclude that noise in the divider, which supplies LO to the quads, can be ignored.

In contrast with the technique used in [2], which requires high LO voltage swings and matching between the dc and dynamic PMOS injected currents, the technique proposed here is robust over PVT and offers several additional benefits as discussed above. The disadvantage compared to [2] is that our technique requires a higher supply voltage.

The mixer is fabricated in a 0.13µm CMOS technology with a 2.7V power supply. A clock tree that includes dividers and buffers for multi-band operation drives the mixer. Performance at 1960MHz, extrapolated from receiver measurements, is summarized in Fig. 25.8.6. The total I/Q mixer current is 3mA and the 2*LO buffer uses 3mA of current. In the conventional mixer design, quad devices optimized for 1/*f* noise are about 5 times larger in area. The noise figure at 10kHz offset improves from 18dB to 8.5dB. The thermal noise floor at 1MHz improves by 2dB. The measured gain for our mixer is 2dB higher than a conventional mixer. IIP2 measurements for the new mixer indicate typical values in the range of 60 to 70dBm. This topology results in a small die area increase of 30×40µm², mainly due to the extra buffer used in the 2*LO path.

References:

[1] M. T. Terrovitis and R. G. Meyer, "Noise in Current-Commutating CMOS Mixers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 772-783, June, 1999.

[2] H. Darabi and J. Chu, "A Noise Cancellation Technique in Active RF-CMOS Mixers," *IEEE ISSCC Dig. Tech. Papers*, pp. 544-545, Feb., 2005.

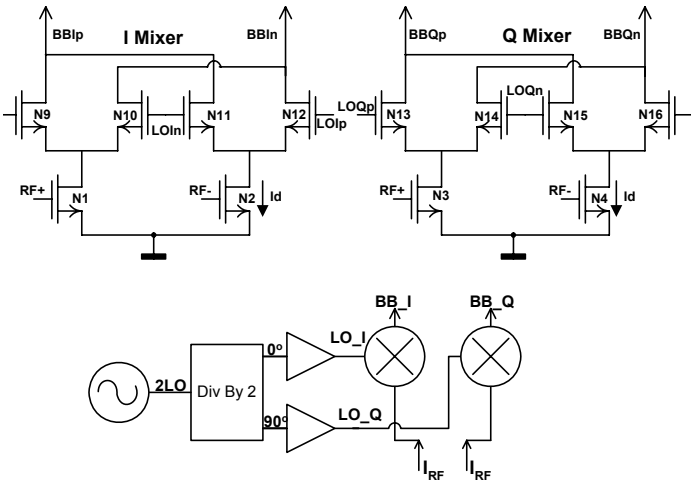

Figure 25.8.1: Conventional quadrature mixer topology.

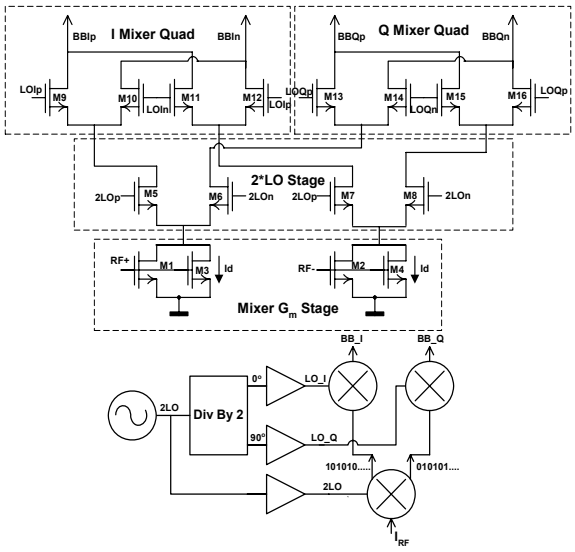

Figure 25.8.2: Quadrature mixer topology.

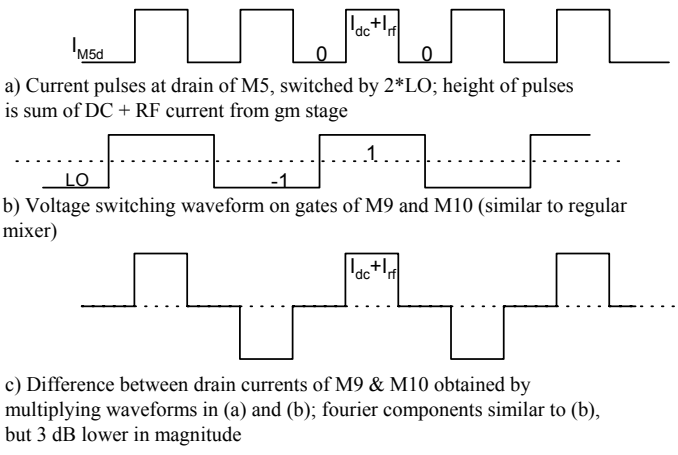

Figure 25.8.3: Waveforms for quadrature mixer topology.

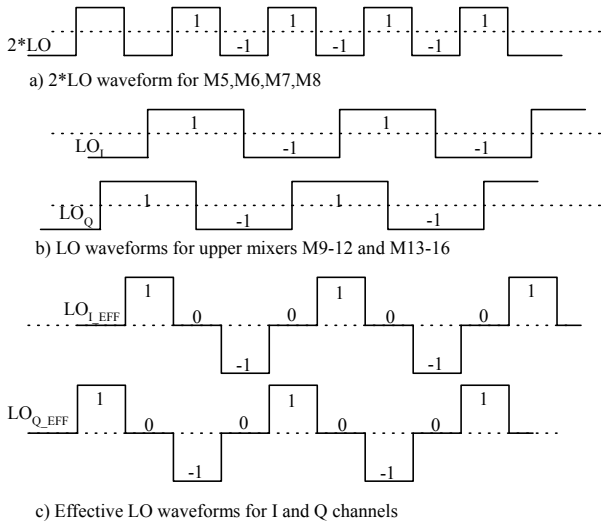

Figure 25.8.4: Effective switching waveforms for quadrature mixer topology.

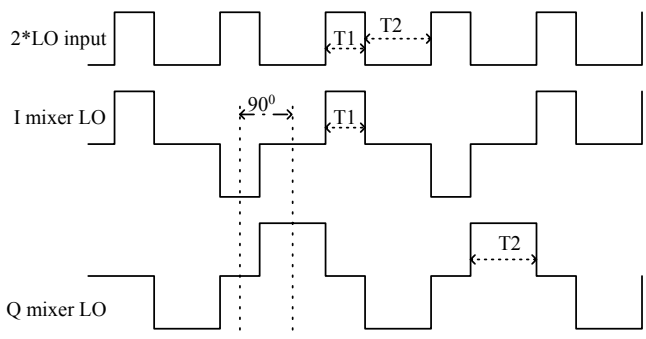

Figure 25.8.5: Clock duty cycle mismatch converts to quadrature amplitude error and negligible phase error.

	Our Mixer		Conventional Mixer	
	Measured	Simulated	Measured	Simulated
Voltage Gain with 200Ohm resistor @ mixer output	7 dB	8.5 dB	5 dB	6 dB
IIP3	2 dBm	4 dBm	1 dBm	4 dBm
NF at 10KHz offset	8.5 dB	7 dB	18 dB	19.5 dB
NF at 1MHz offset	6.5 dB	5.5 dB	8.5 dB	8.0 dB
Current (I_d as shown in fig. 1 & fig. 2)	0.75 mA	0.75 mA	0.75 mA	0.75 mA

Figure 25.8.6: Summary of measured and simulated results.

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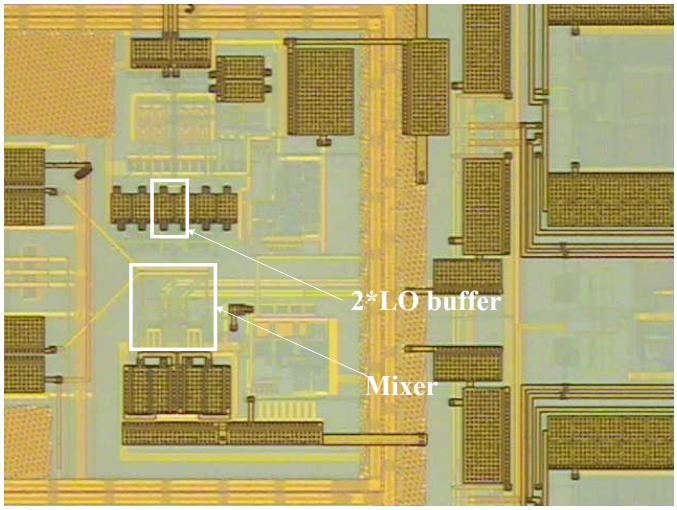

Figure 25.8.7: Chip micrograph.

